IN THE CLAIMS:

Please find below a listing of all of the pending claims. The statuses of the claims are set forth in parentheses.

Claims 1-6 (Canceled).

7. (Currently Amended) A memory cell comprising:

a diffusive metal gate electrode;

at least one floating gate;

a gate insulator including a first gate insulator layer disposed between the at least one floating gate and the diffusive metal gate electrode, and a second gate insulator disposed below and coupled to the first gate insulator layer;

a channel region coupled to the gate insulator;

a source coupled to the channel region;

a drain coupled to the channel region; and

a diffused metal path connecting the diffusive metal gate electrode to the at least one floating gate.

~~wherein the first gate insulator layer includes a conductive path formed by the diffusion of conductive elements from the diffusive metal through the gate insulator in response to a write voltage applied to the diffusive metal, and the at least one floating gate adapted to prevent the conductive elements from the diffusive metal from diffusing into the second gate insulator layer.~~

8. (Original) The memory cell of claim 7, wherein the channel region, the source and the drain are parts of a continuous layer of semiconductor material.

9. (Original) The memory cell of claim 8, wherein the source and drain are doped regions of the layer of semiconductor material.

10. (Canceled).

11. (Canceled).

12. (Previously Presented) The memory cell of claim 7, wherein the at least one floating gate comprises a plurality of floating gates, and wherein the gate insulator comprises a plurality of gate insulator layers extending between the floating gates.

13. (Currently Amended) A memory array, comprising:

a substrate;

a plurality of gates lines disposed over the substrate;

a plurality of data lines crossing the gate lines and disposed over the substrate; and

a plurality of memory cells at crossing points of the gate lines and the data lines, each memory cell being coupled to a gate line and a data line that cross at the memory cell, wherein a memory cell comprises:

a diffusive metal gate electrode;

at least one floating gate;

a gate insulator including a first gate insulator layer disposed between the at least one floating gate and the diffusive metal gate electrode, and a second gate insulator disposed below and coupled to the first gate insulator layer;

a channel region coupled to the gate insulator;

a source coupled to the channel region;

a drain coupled to the channel region; and

a diffused metal path connecting the diffusive metal gate electrode to the at least one floating gate.

~~wherein the first gate insulator layer includes a conductive path formed by the diffusion of conductive elements from the diffusive metal through the gate insulator in response to a write voltage applied to the diffusive metal, and the at least one floating gate adapted to prevent the conductive elements from the diffusive metal from diffusing into the second gate insulator layer.~~

14. (Original) The memory array of claim 13, wherein the data lines comprise strips of semiconductor material, the sources and the drains comprising doped regions of the data lines.

15. (Currently Amended) The memory array of claim 13, wherein the gate insulator extends between the diffusive metal gate electrode and the floating gate, and between the floating gate and the channel region.

16. (Currently Amended) The memory array of claim 13, wherein the gate lines are conductive lines coupled to the memory cells, the diffusive metal gate electrode comprising a part of a gate line.

17. (Original) The memory array of claim 13, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.

18. (Original) The memory array of claim 13, wherein the gate lines comprise: a first conductor disposed over the gate insulator; and a second conductor coupled to the first conductor.

19. (Original) The memory array of claim 18, wherein the first conductor includes a diffusive metal disposed between the insulator and the second conductor.

20. (Original) The memory array of claim 13, wherein the substrate comprises at least one of a glass or a plastic.

Claims 21-25 (Canceled).

26. (Currently Amended) A memory cell, comprising:

a diffusive metal gate electrode;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal gate electrode, ~~wherein~~ the gate insulator comprisinges a low temperature oxide ~~and a conductive path formed from conductive elements from the diffusive metal diffused through the gate insulator in response to a write voltage applied to the diffusive metal~~;

a diffused metal path within the gate insulator and connecting the diffusive metal gate electrode to the at least one floating gate;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region.

27. (Previously Presented) The memory cell of claim 26, wherein the channel region, the source, and the drain are parts of a continuous layer of semiconductor material.

28. (Previously Presented) The memory cell of claim 27, wherein the source and drain are doped regions of the layer of semiconductor material.

29. (Currently Amended) The memory cell of claim 26, wherein the gate insulator extends between the diffusive metal gate electrode and the at least one floating gate and the channel region.

30. (Canceled).

31. (Previously Presented) The memory cell of claim 26, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.

32. (Currently Amended) The memory cell of claim ~~1~~ 7, wherein ~~specification,~~ the at least one floating gate comprises a metal selected from the group consisting of W, Al, Cr, TiW, and Cu.

33. (New) The memory cell of claim 7, wherein the diffused metal path is formed by the diffusion of conductive elements from the diffusive metal gate electrode through the gate insulator in response to a write voltage applied to the diffusive metal gate electrode.

34. (New) The memory cell of claim 33, wherein the diffused metal path is broken by the diffusion of conductive elements towards the diffusive metal gate electrode in response to a reversal of the write voltage applied to the diffusive metal gate electrode.

35. (New) The memory cell of claim 7, wherein the at least one floating gate is adapted to prevent the conductive elements from the diffusive metal gate electrode from diffusing into the second gate insulator layer.

36. (New) The memory cell of claim 13, wherein the diffused metal path is formed by the diffusion of conductive elements from the diffusive metal gate electrode through the gate insulator in response to a write voltage applied to the diffusive metal gate electrode.

37. (New) The memory cell of claim 36, wherein the diffused metal path is broken by the diffusion of conductive elements towards the diffusive metal gate electrode in response to a reversal of the write voltage applied to the diffusive metal gate electrode.

38. (New) The memory cell of claim 13, wherein the at least one floating gate is adapted to prevent the conductive elements from the diffusive metal gate electrode from diffusing into the second gate insulator layer.

39. (New) The memory cell of claim 26, wherein the diffused metal path is formed by the diffusion of conductive elements from the diffusive metal gate electrode through the gate insulator in response to a write voltage applied to the diffusive metal gate electrode.

40. (New) The memory cell of claim 39, wherein the diffused metal path is broken by the diffusion of conductive elements towards the diffusive metal gate electrode in response to a reversal of the write voltage applied to the diffusive metal gate electrode.

41. (New) The memory cell of claim 29, wherein the at least one floating gate is adapted to prevent the conductive elements from the diffusive metal gate electrode from diffusing into the gate insulator between the at least one floating gate and the channel region.